



SYSTEM BUS 431

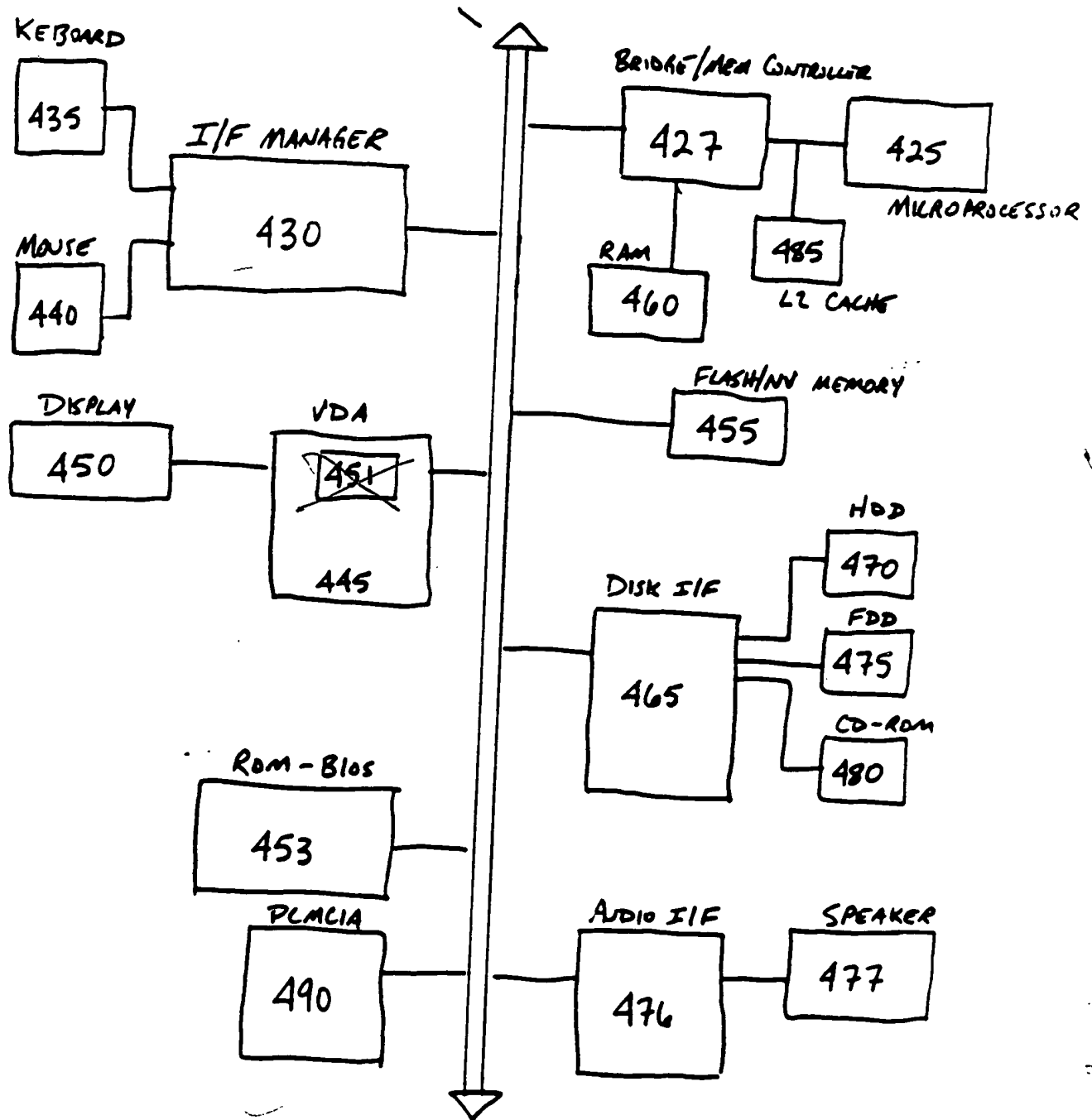


FIG 1



7D-152

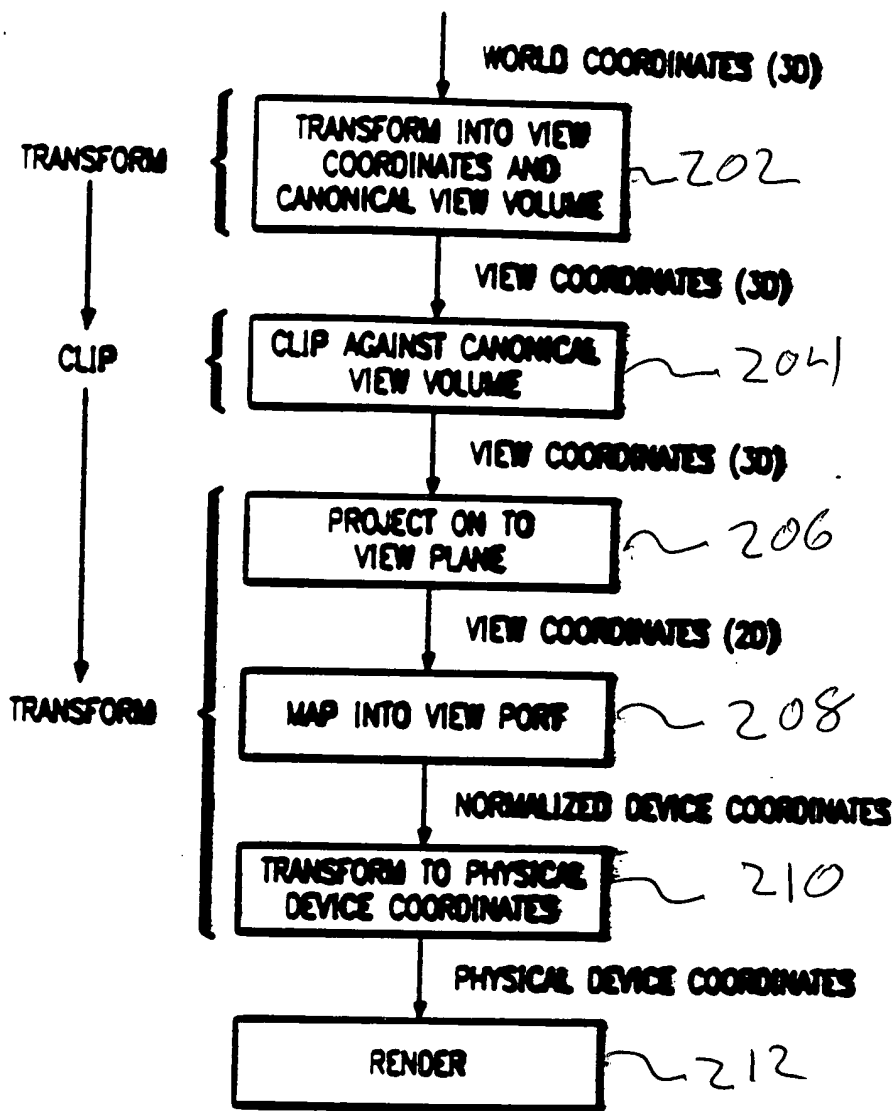


FIG. 2



TP-152

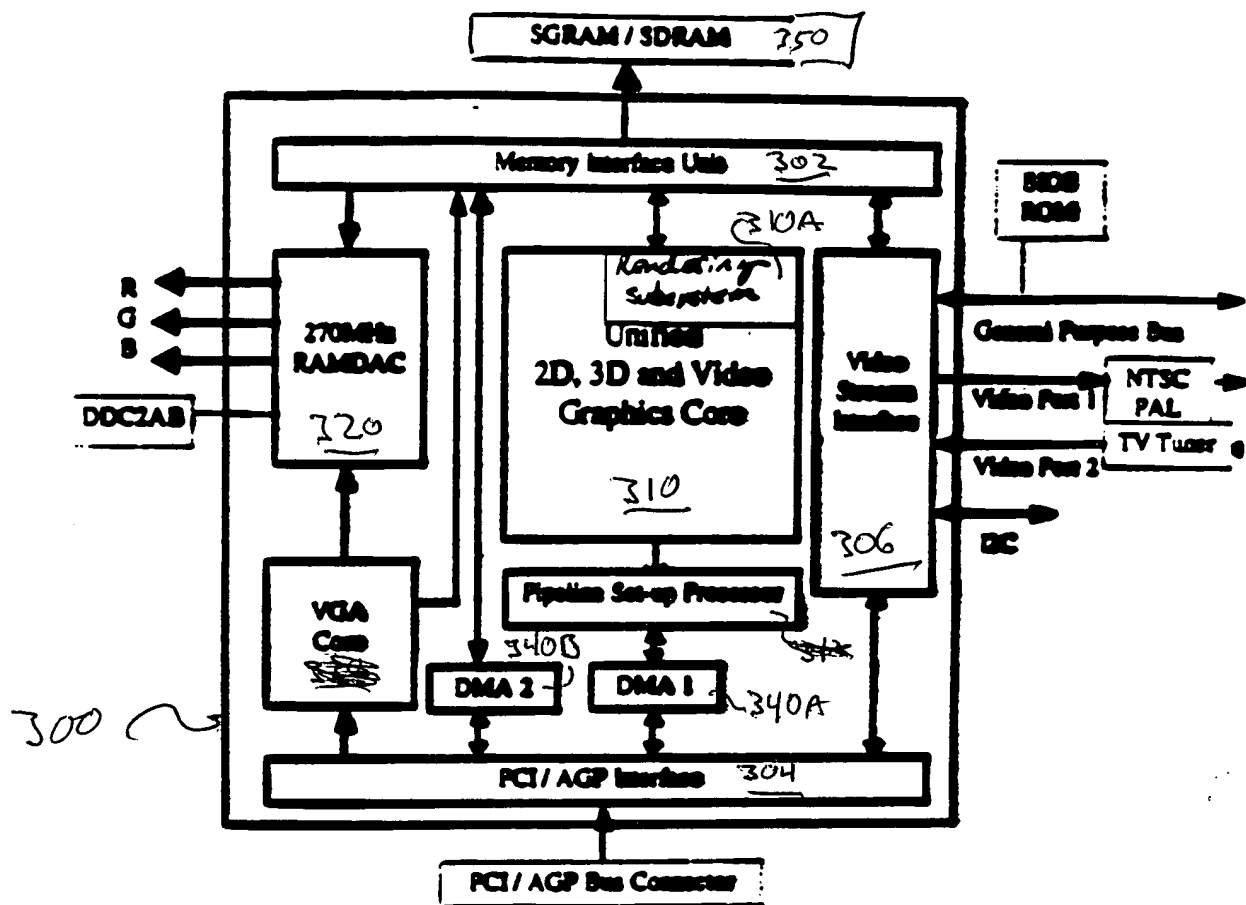


Figure 3

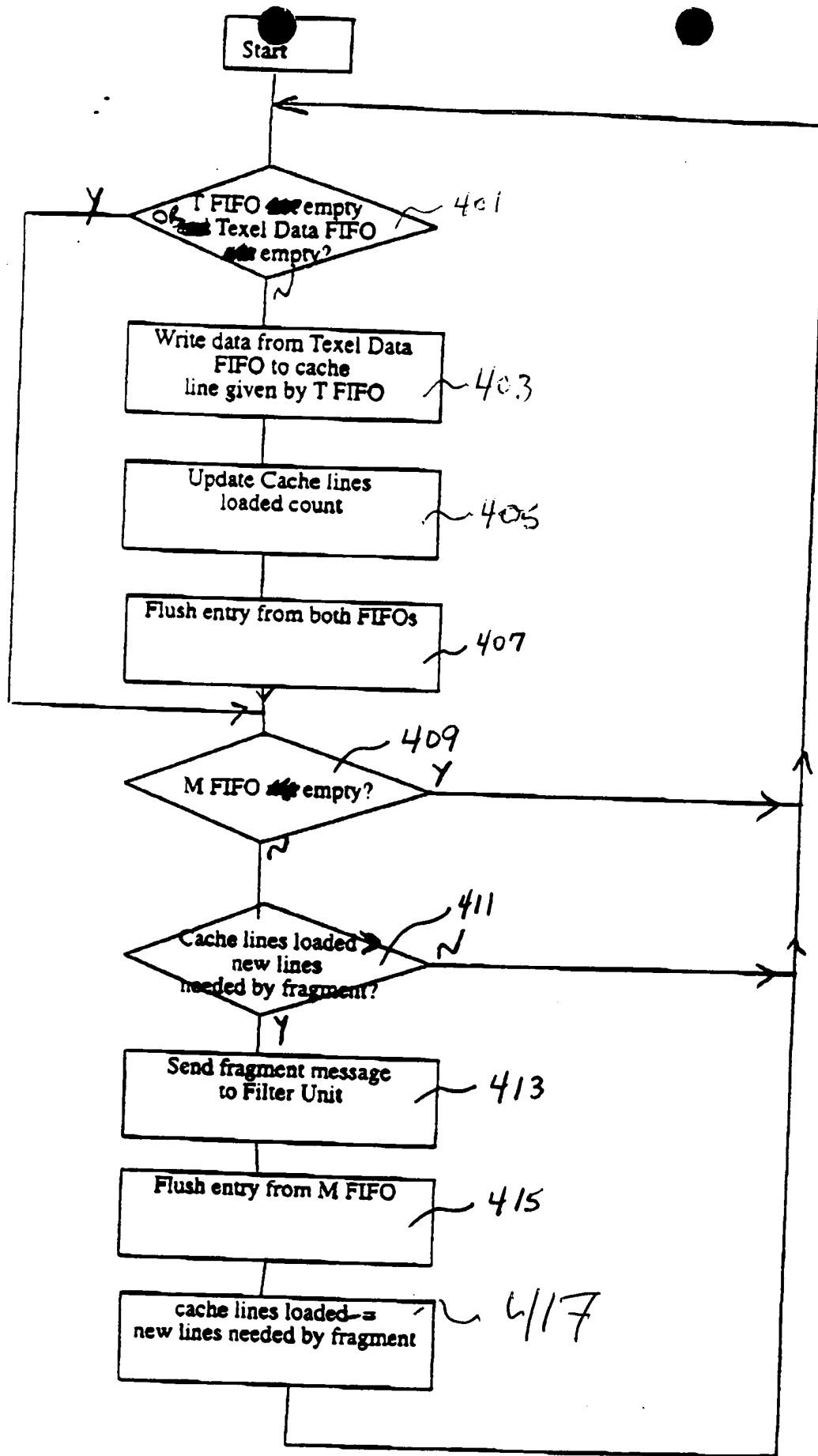


FIG. 4A



TD-152

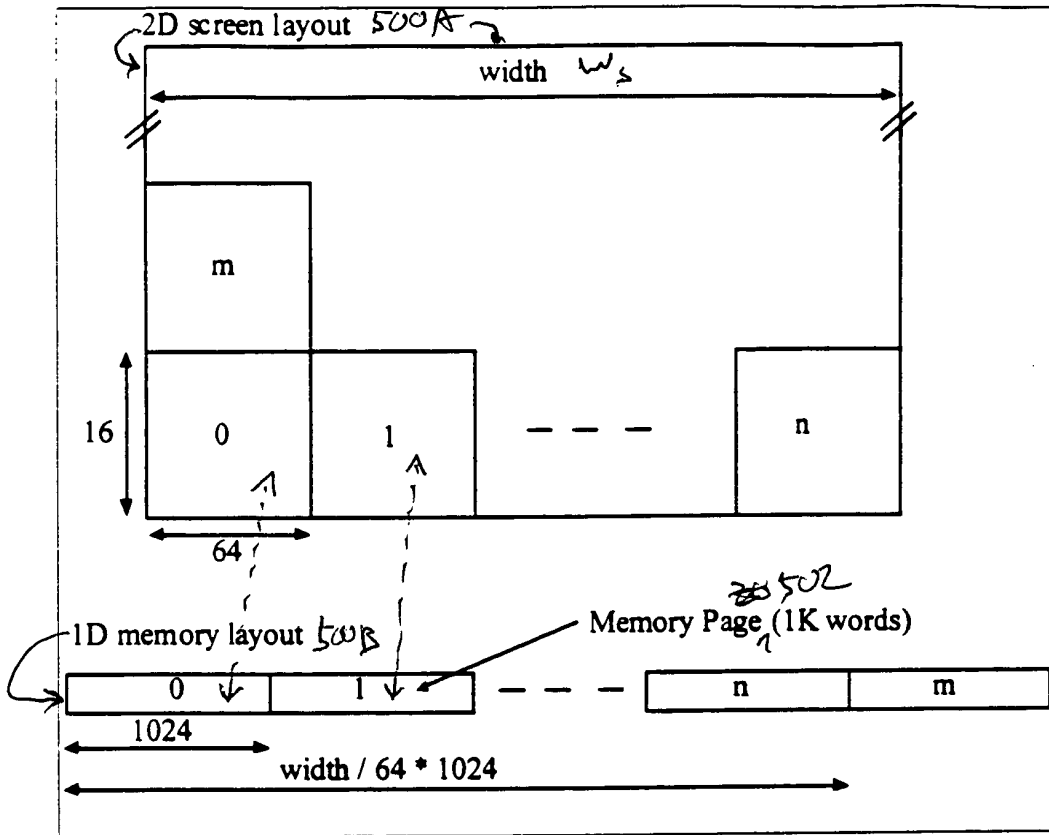


FIG. 5

Texture Map 600

Filler
res. size
255.596
602
Texture
codes
604

	T0	T1	T0	T1	T0	T1	T0	T1	T0	T1
	(0,4)	(1,4)	(2,4)	(3,4)	(4,4)	(5,4)	(6,4)	(7,4)	(8,4)	(9,4)
	T2	T3	T2	T3	T2	T3	T2	T3	T2	T3
	(0,3)	(1,3)	(2,3)	(3,3)	(4,3)	(5,3)	(6,3)	(7,3)	(8,3)	(9,3)
	T0	T1	T0	T1	T0	T1	T0	T1	T0	T1
	(0,2)	(1,2)	(2,2)	(3,2)	(4,2)	(5,2)	(6,2)	(7,2)	(8,2)	(9,2)
	T0	T1	T0	T1	T0	T1	T0	T1	T0	T1
	(0,1)	(1,1)	(2,1)	(3,1)	(4,1)	(5,1)	(6,1)	(7,1)	(8,1)	(9,1)
	T0	T1	T0	T1	T0	T1	T0	T1	T0	T1
	(0,0)	(1,0)	(2,0)	(3,0)	(4,0)	(5,0)	(6,0)	(7,0)	(8,0)	(9,0)

610 612 614

- 32 bit texels in memory word (610)
- 16 bit texels in memory word (612)
- 8 bit texels in memory word (614)

FIG. 6



Linear or Patch64 Memory Layouts

32 bits per texel (byout 702)

120	112	104	96	88	80	72	64	56	48	40	32	24	16	8	0
(3, 0)				(2, 0)				(1, 0)				(0, 0)			

16 bits per texel (byout 704)

120	112	104	96	88	80	72	64	56	48	40	32	24	16	8	0
(7, 0)	(6, 0)	(5, 0)	(4, 0)	(3, 0)	(2, 0)	(1, 0)	(0, 0)								

8 bits per texel (byout 706)

120	112	104	96	88	80	72	64	56	48	40	32	24	16	8	0
(15, 0)	(14, 0)	(13, 0)	(12, 0)	(11, 0)	(10, 0)	(9, 0)	(8, 0)	(7, 0)	(6, 0)	(5, 0)	(4, 0)	(3, 0)	(2, 0)	(1, 0)	(0, 0)

FIG. 7A

Patch32_2 or Patch2 Memory Layouts

32 bits per texel (byout 712)

120	112	104	96	88	80	72	64	56	48	40	32	24	16	8	0
(1, 1)				(0, 1)				(1, 0)				(0, 0)			

16 bits per texel (byout 714)

120	112	104	96	88	80	72	64	56	48	40	32	24	16	8	0
(3, 1)	(2, 1)	(3, 0)	(2, 0)	(1, 1)	(0, 1)	(1, 0)	(0, 0)								

8 bits per texel (byout 716)

120	112	104	96	88	80	72	64	56	48	40	32	24	16	8	0
(7, 1)	(6, 1)	(7, 0)	(6, 0)	(5, 1)	(4, 1)	(5, 0)	(4, 0)	(3, 1)	(2, 1)	(3, 0)	(2, 0)	(1, 1)	(0, 1)	(1, 0)	(0, 0)

FIG. 7B

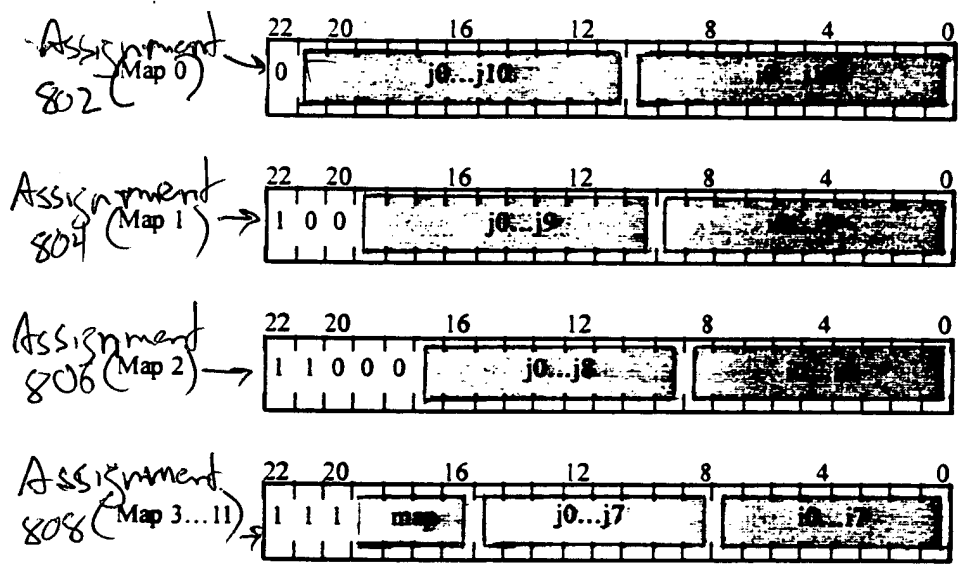


FIG. 8

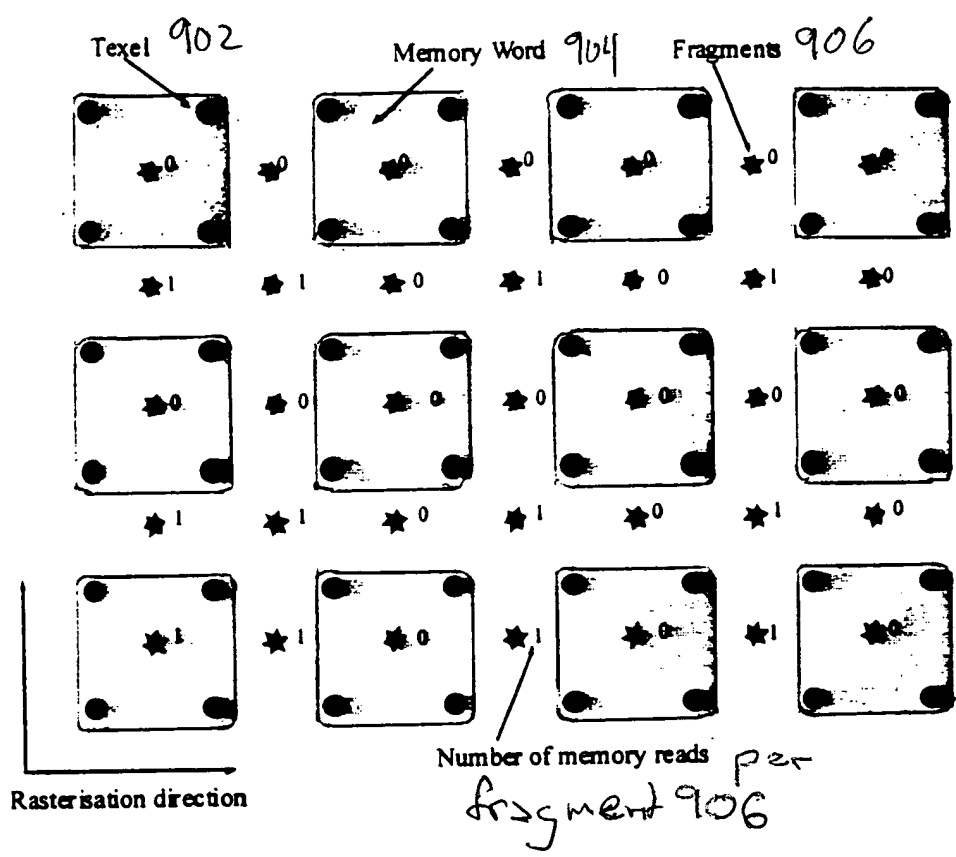


FIG. 9

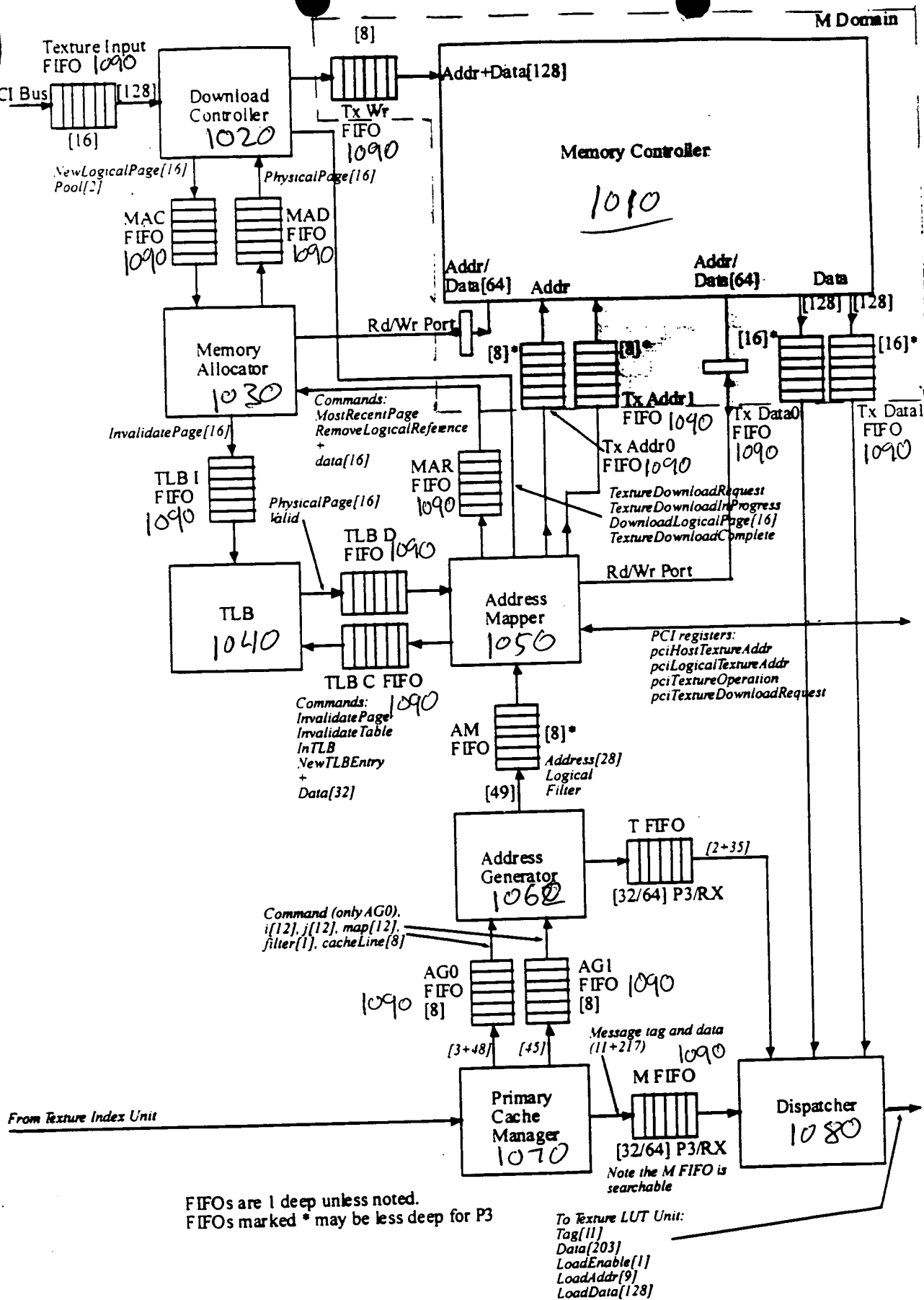


FIG. 10

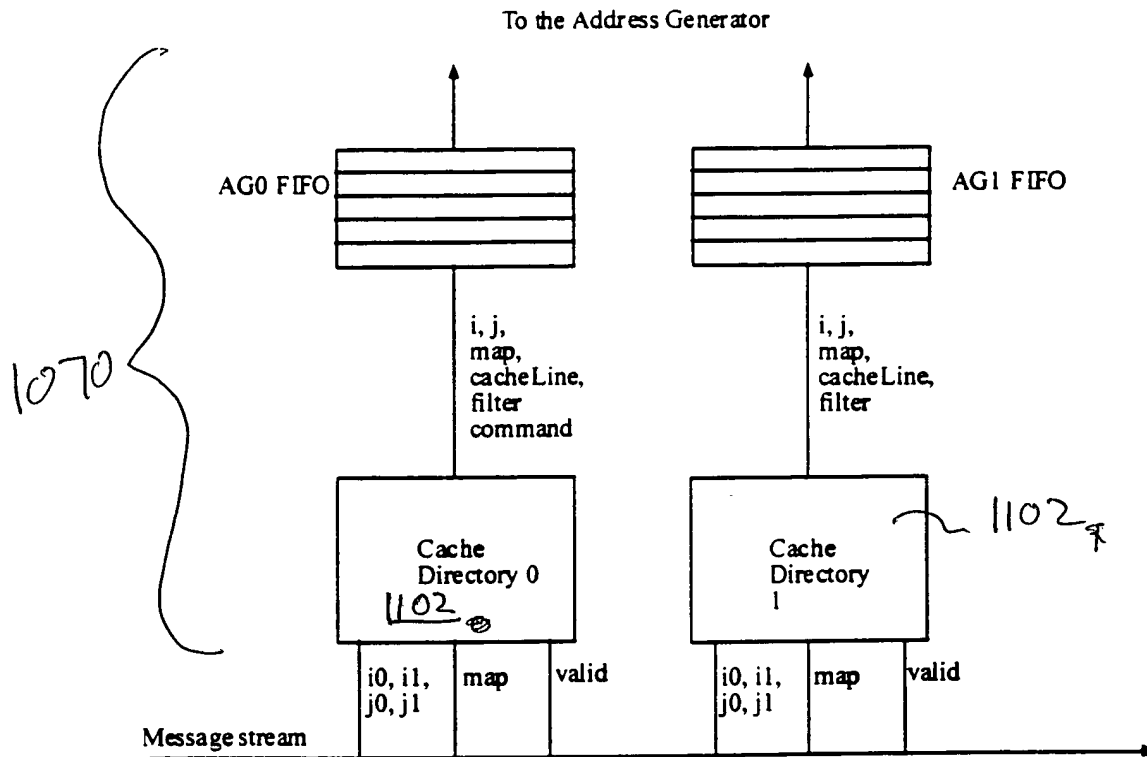


FIG. 11

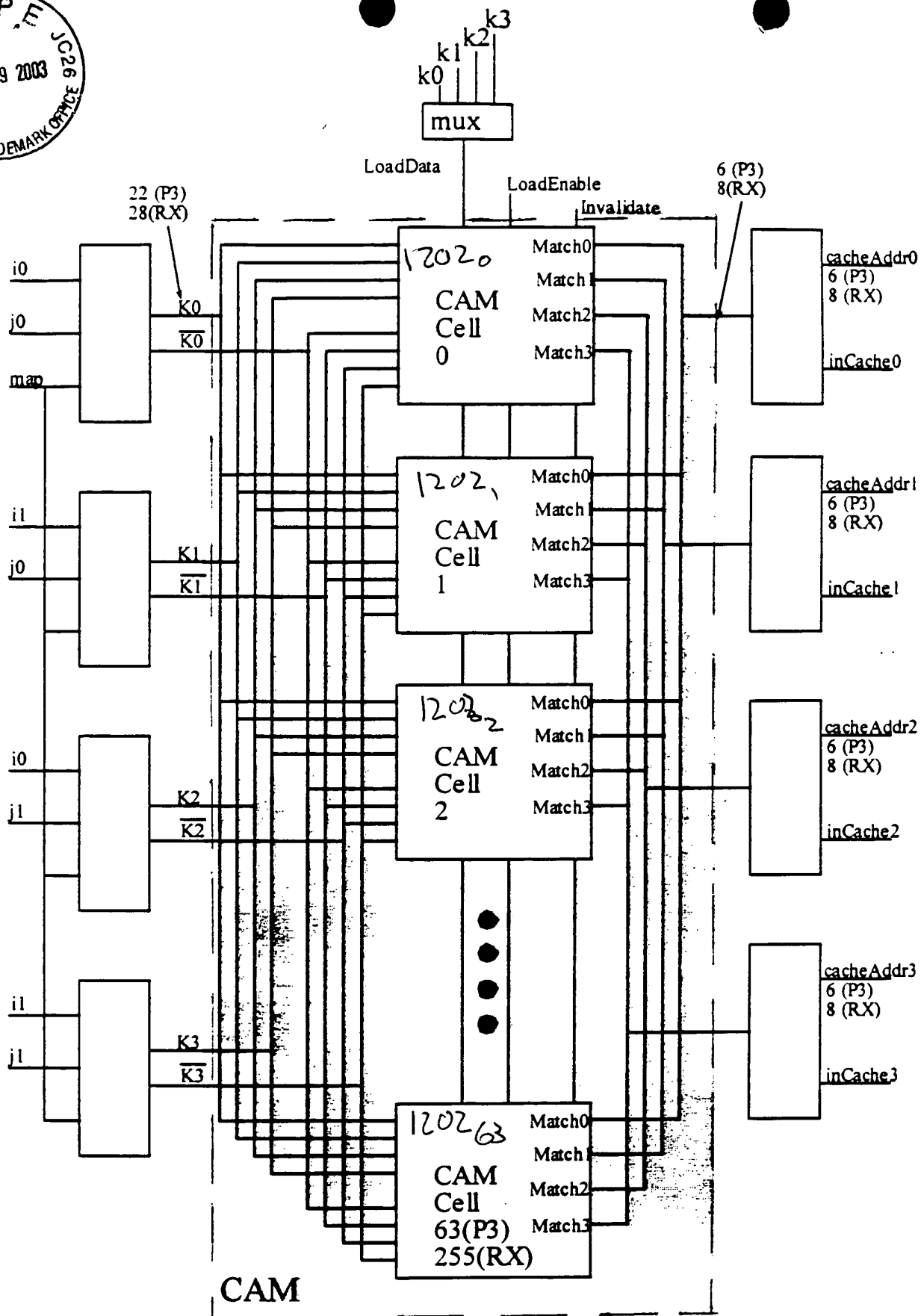


FIG 12



1202

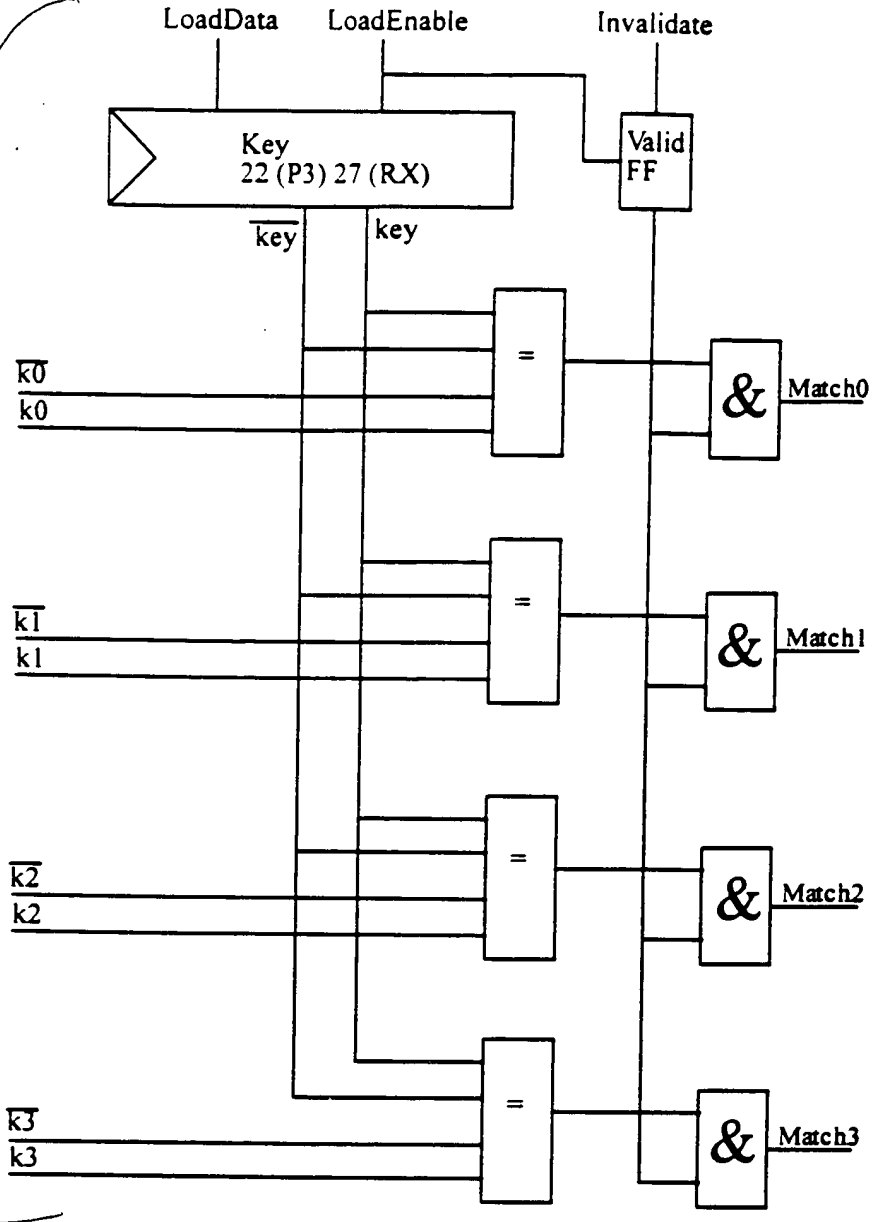


FIG. 13



TLB 1040

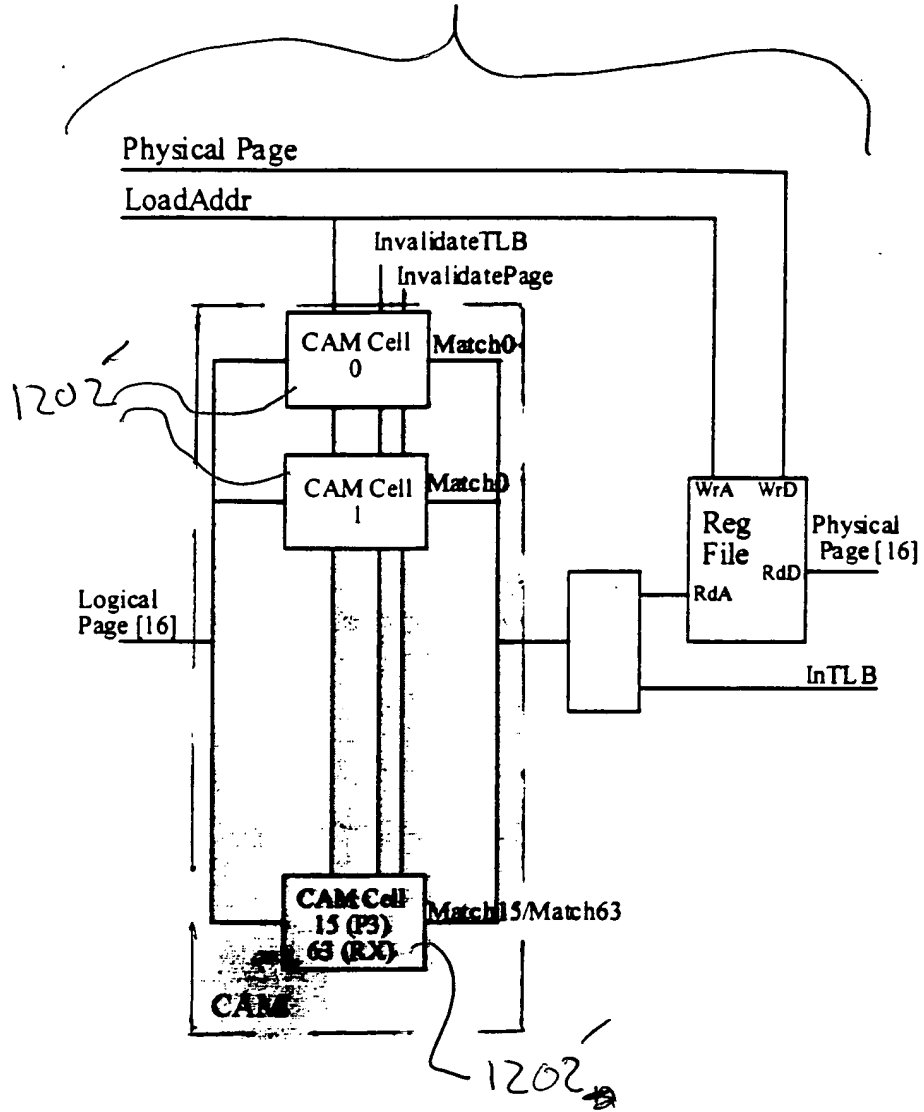


FIG. 14



1202

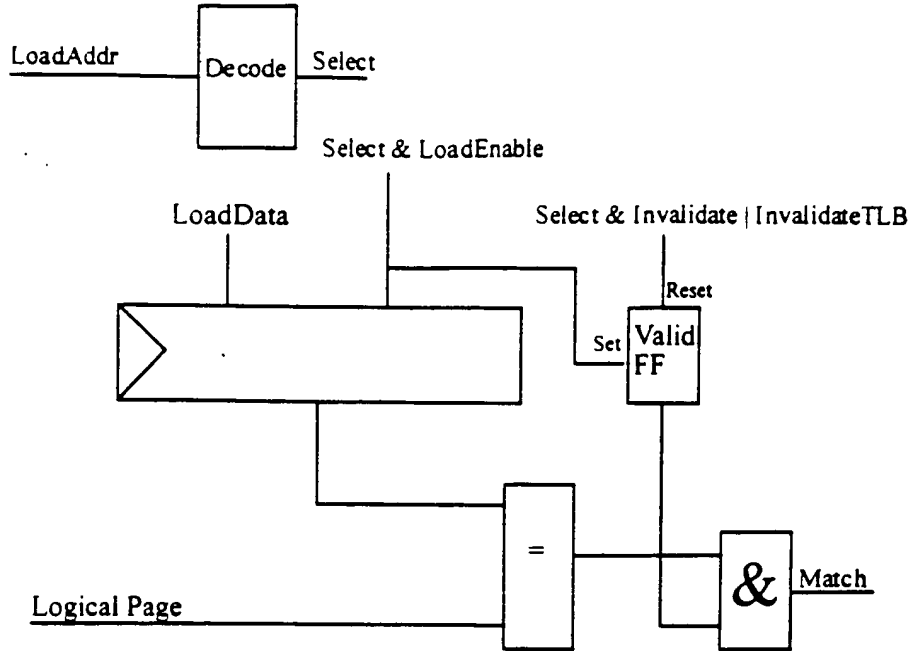


FIG. 15



TD-152

CPUs

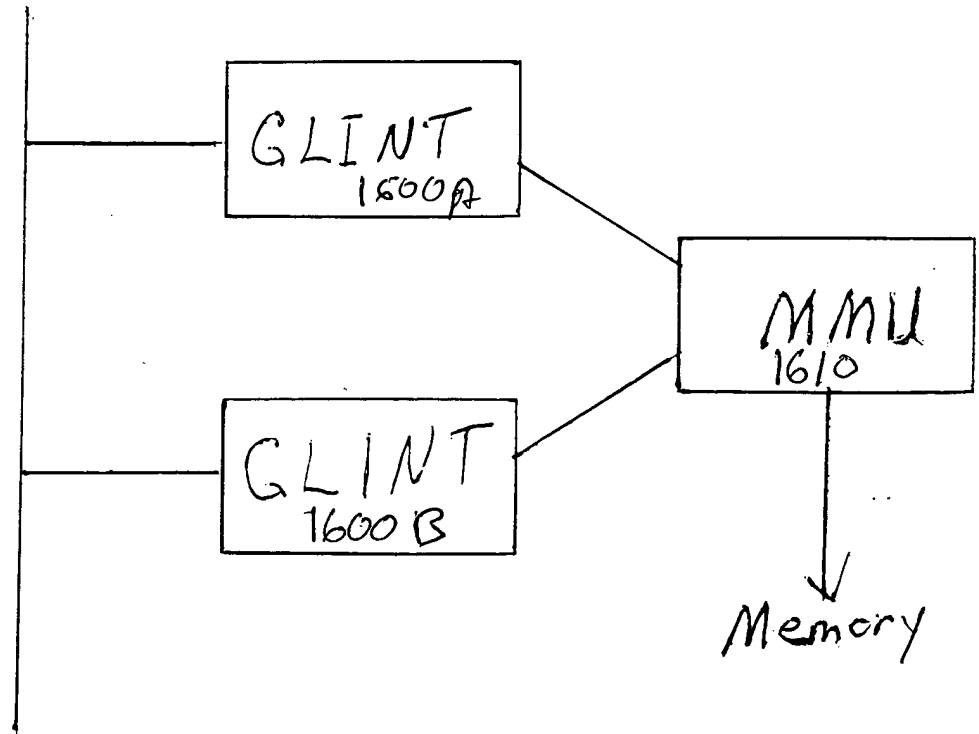


FIG. 16